

4-Line Ultra Low Capacitance TVS Diode Array

Features

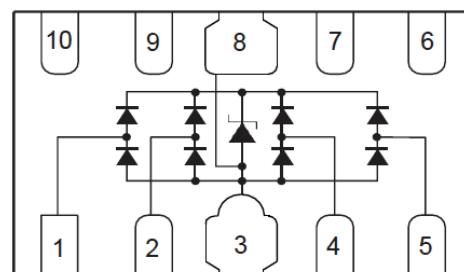
- IEC 61000-4-2 (ESD) $\pm 25\text{kV}$ (air), $\pm 20\text{kV}$ (contact)
- IEC 61000-4-5 (Lightning) 5A (8/20 μs)
- Ultra low Capacitance: 0.25pF typical (I/O to I/O)
- Ultra low leakage: nA level
- Operating Voltage: 5V
- Low clamping Voltage
- Up to 4 lines protects

Applications

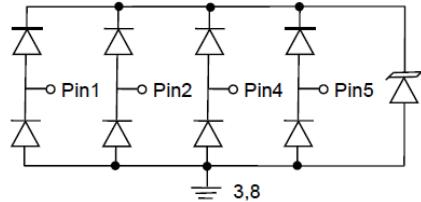
- HDMI 1.3/1.4/2.0, USB 2.0/3.0 and MDDI ports
- Monitors and flat panel displays
- Set-top box and Digital TV
- Video graphics cards
- Digital Visual Interface (DVI)
- Notebook Computers
- PCI Express and serial SATA ports

Mechanical Characteristics

- Package: DFN2510-10L ($2.5 \times 1.0 \times 0.5\text{mm}$)
- Lead Finish: Matte Tin
- Case Material: "Green" Molding Compound.
- Moisture Sensitivity: Level 3 per J-STD-020
- RoHS Compliant

Schematic & PIN ConfigurationDFN2510-10L
(Top View)

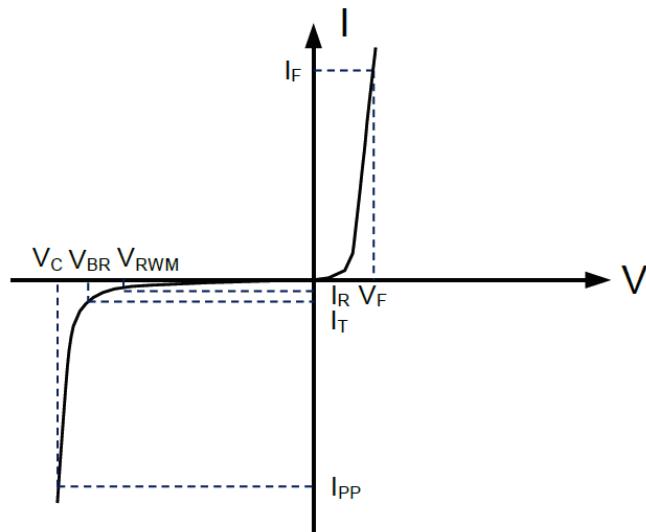
Pin	Identification
1,2,4,5	Input Lines
6,7,9,10	Output Lines (No Internal Connection)
3,8	Ground

Circuit Diagram**Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless otherwise noted)**

Parameter	Symbol	Value	Unit
Peak Pulse Power ($tp = 8/20\mu\text{s}$)	P_{PP}	60	W
Peak Pulse Current ($tp = 8/20\mu\text{s}$)	I_{PP}	5	A
ESD per IEC 61000-4-2 (Air)	V_{ESD}	± 25	kV
ESD per IEC 61000-4-2 (Contact)		± 20	kV
Operating Temperature Range	T_J	-55 to + 125	°C
Storage Temperature Range	T_{STG}	-55 to + 150	°C

Electrical Parameters ($T_A = 25^\circ\text{C}$ Unless otherwise noted)

Symbol	Parameter
I_{PP}	Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Reverse Working Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F

Electrical Characteristics ($T_A = 25^\circ\text{C}$ Unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Reverse Working Voltage	V_{RWM}	Any I/O pin to ground			5	V
Reverse breakdown Voltage	V_{BR}	$I_T = 1\text{mA}$, any I/O pin to ground	6			V
Reverse leakage current	I_R	$V_{RWM} = 5\text{V}$, any I/O pin to ground			0.2	μA
Forward Voltage	V_F	$I_F = 10\text{mA}$, ground to any I/O pin		0.9	1.1	V
Clamping Voltage	V_C	$I_{PP} = 1\text{A}$ ($t_p = 8/20\mu\text{s}$), any I/O pin to ground		7.5	9	V
Clamping Voltage	V_C	$I_{PP} = 5\text{A}$ ($t_p = 8/20\mu\text{s}$), any I/O pin to ground		9	12	V
Junction capacitance	C_J	$V_R = 0\text{V}$, $f = 1\text{MHz}$, between I/O pins	0.25	0.4		pF
Junction capacitance	C_J	$V_R = 0\text{V}$, $f = 1\text{MHz}$, any I/O pin to ground	0.5	0.8		pF

Typical Performance Characteristics ($T_A = 25^\circ\text{C}$ Unless otherwise noted)

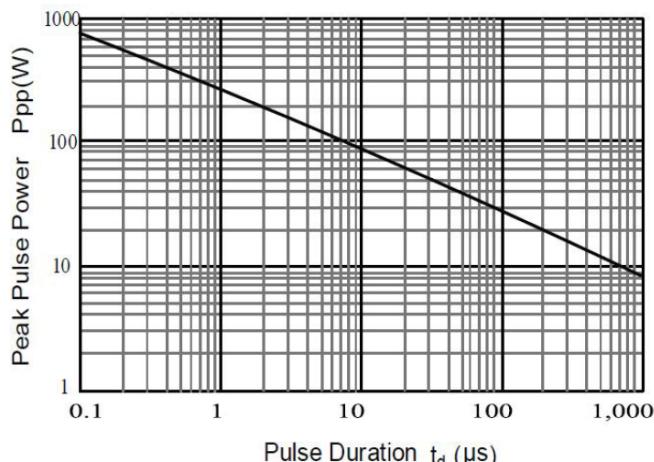


Fig 1. Peak Pulse Power vs. Pulse Time

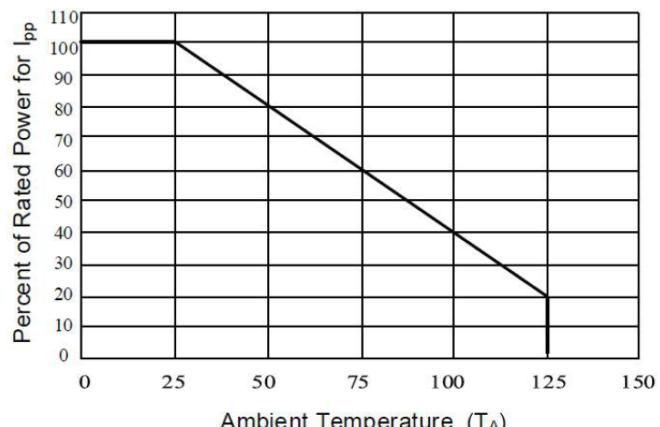


Fig 2. Power Derating Curve

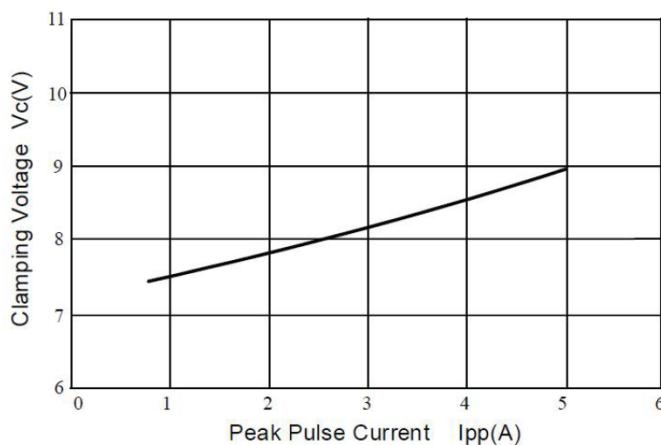


Fig 3. Clamping Voltage vs. Peak Pulse Current

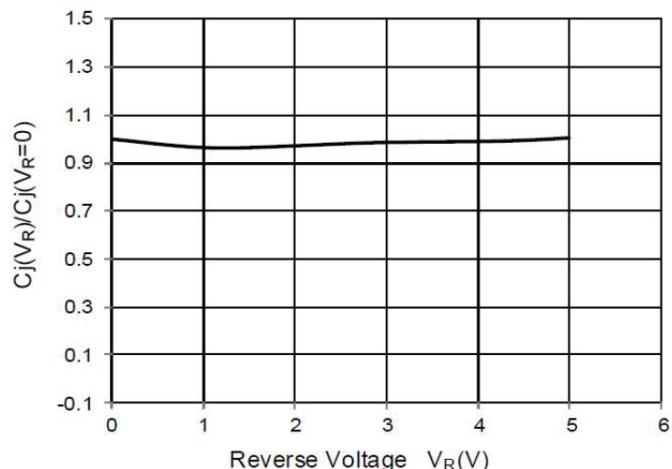


Fig 4. Junction Capacitance vs. Reverse Voltage

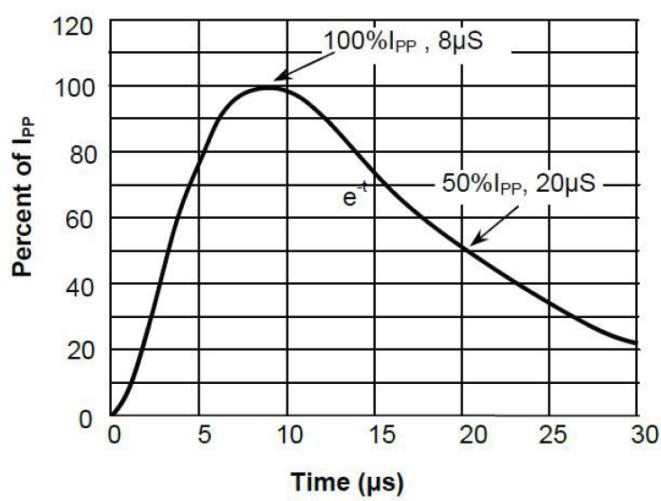


Fig 5. 8/20 μs Pulse Waveform

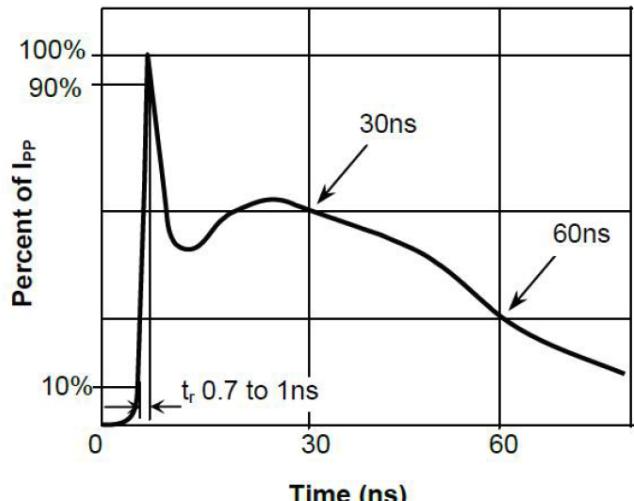


Fig 6. ESD(IEC 61000-4-2)Pulse Waveform

DFN2510-10L Package Outline Drawing

Symbol	DIMENSIONS					
	(mm)			(inch)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.450	0.500	0.600	0.018	0.020	0.024
A1	0.000	0.020	0.050	0.000	0.001	0.002
b	0.150	0.200	0.250	0.006	0.008	0.010
b1	0.350	0.400	0.450	0.014	0.016	0.018
b2	0.200	0.250	0.300	0.008	0.010	0.012
c	0.100	0.150	0.200	0.004	0.006	0.008
D	2.450	2.500	2.550	0.098	0.100	0.102
e	0.50 BSC			0.020 BSC		
Nd	2.00 BSC			0.080 BSC		
E	0.950	1.000	1.050	0.038	0.040	0.042
L	0.350	0.400	0.450	0.014	0.016	0.018
L1	0.075 REF			0.003 REF		
L2	0.050 REF			0.002 REF		
R	0.050	0.100	0.150	0.002	0.004	0.006

The package outline drawings show the physical dimensions of the DFN2510-10L package. The Top View shows the overall width (D) and height (E). The Side View shows the thickness (A), lead spacing (e), and lead height (Nd). The Bottom View shows the lead profile with lead width (b), lead pitch (b1+b2), lead height (Nd), lead thickness (R), and lead offset (L).

Suggested PAD Layout

Symbol	DFN2510-10L		X1	X2	Y	Z
	(mm)	(inch)				
X1	0.200	0.008				
X2	0.400	0.016				
X3	0.500	0.020				
Y	0.600	0.024				
Z	1.400	0.056				

The suggested PAD layout shows the placement of pads on the package. The layout consists of two rows of pads. The first row has three pads with width X1 and height Y. The second row has four pads with width X2 and height Y. The total width between the outermost pads is X3. The height of the package is Z.

Ordering information

Part Number	Package	Marking Code	Base qty	Reel Size	Delivery mode
			(pcs)	(inch)	
STCDN524BL	DFN2510-10L	0524B	3,000	7	Tape and reel