

Bi-directional 12V Low Capacitance ESD Protector

Features

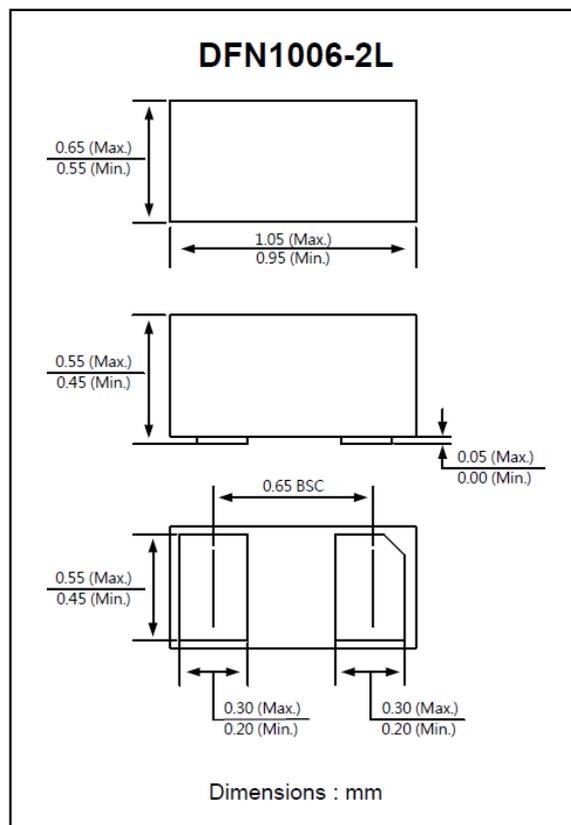
- IEC 61000-4-2 (ESD) $\pm 20\text{kV}$ (air), $\pm 20\text{kV}$ (contact)
- IEC 61000-4-5 (Lightning) 2.5A (8/20 μs)
- Low capacitance 0.25pF typical
- Ultra low leakage: nA level
- Low clamping voltage
- Operating voltage : 12V
- 2-pin leadless package

Applications

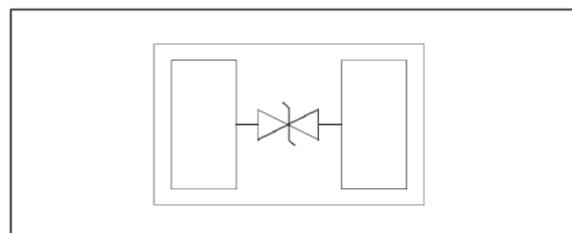
- Cell phone Handsets and Accessories
- PCI Express and Serial SATA Ports
- Display Ports
- MDDI Ports
- Peripherals
- Digital Visual Interface (DVI)

Mechanical Characteristics

- Package: DFN1006-2 (1.0 \times 0.6 \times 0.5mm)
- Case Material: "Green" Molding Compound.
- Moisture Sensitivity: Level 3 per J-STD-020
- RoHS compliant



Circuit diagram



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless otherwise noted)

Parameter	Symbol	Value	Unit
Peak Pulse Power ($t_p = 8/20\mu\text{s}$)	P_{PP}	80	W
Peak Pulse Current ($t_p = 8/20\mu\text{s}$)	I_{PP}	2.5	A
ESD per IEC 61000-4-2 (Air)	V_{ESD}	± 20	KV
ESD per IEC 61000-4-2 (Contact)		± 20	KV
Operating Temperature Range	T_J	-55 to + 125	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55 to + 150	$^\circ\text{C}$

Electrical Parameters ($T_A = 25^\circ\text{C}$ Unless otherwise noted)

Symbol	Parameter
V_{RWM}	Reverse Working Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_{PP}	Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}

Electrical Characteristics ($T_A = 25^\circ\text{C}$ Unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Reverse Working Voltage	V_{RWM}				12	V
Reverse breakdown Voltage	V_{BR}	$I_T = 1\text{mA}$	13.5			V
Reverse leakage current	I_R	$V_{RWM} = 12\text{V}$			0.2	μA
Clamping Voltage	V_C	$I_{PP} = 1\text{A}, t_p = 8/20\mu\text{s}$			22	V
Clamping Voltage	V_C	$I_{PP} = 2.5\text{A}, t_p = 8/20\mu\text{s}$			32	V
Junction capacitance	C_J	$V_R = 0\text{V}, f = 1\text{MHz}$		0.25	0.5	pF

Typical Performance Characteristics ($T_A = 25^\circ\text{C}$ Unless otherwise noted)

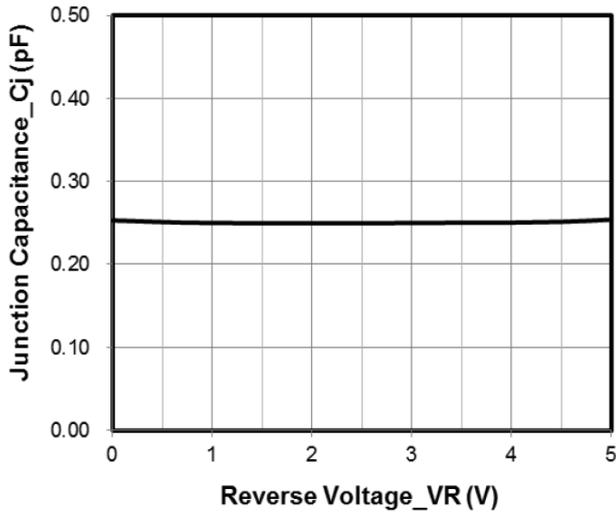


Fig 1. Junction Capacitance vs. Reverse Voltage

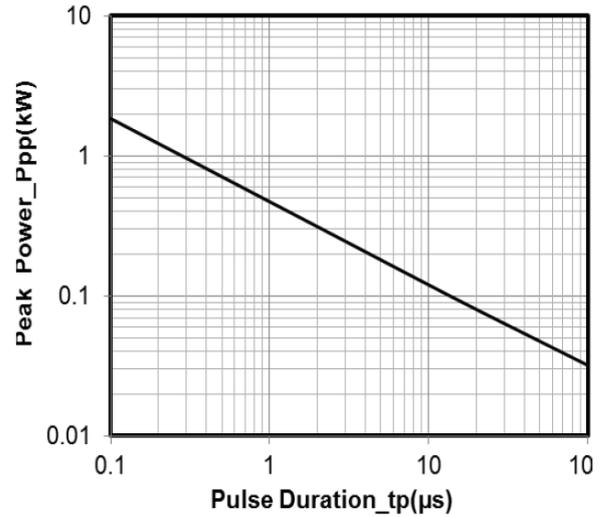


Fig 2. Peak Pulse Power vs. Pulse Time

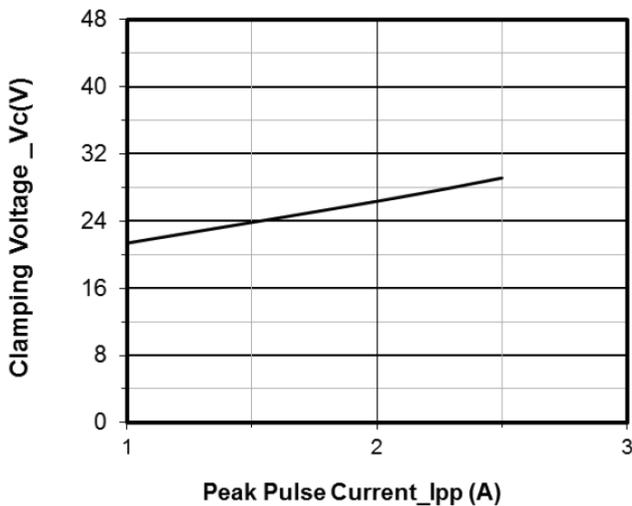


Fig 3. Clamping Voltage vs. Peak Pulse Current

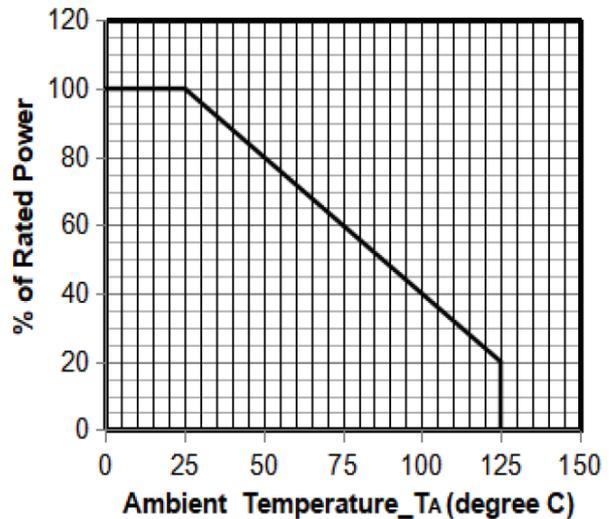


Fig 4. Power Derating Curve

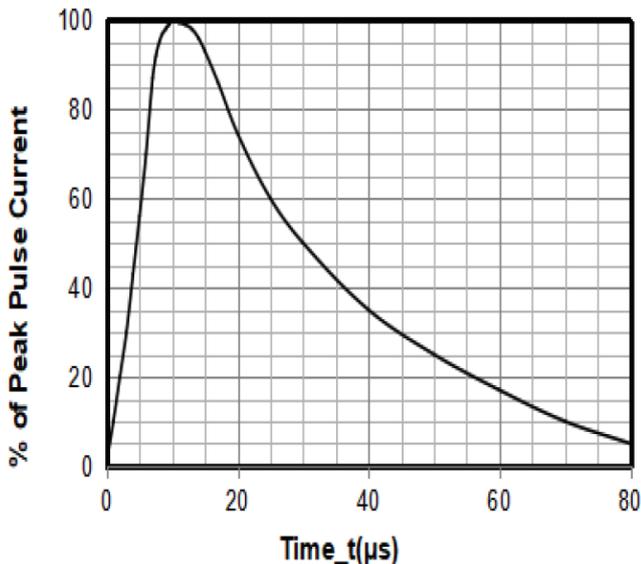
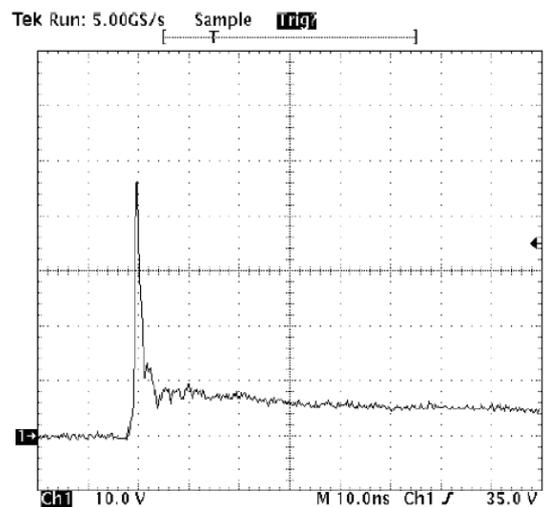


Fig 5. 8 X 20 μs Pulse Waveform

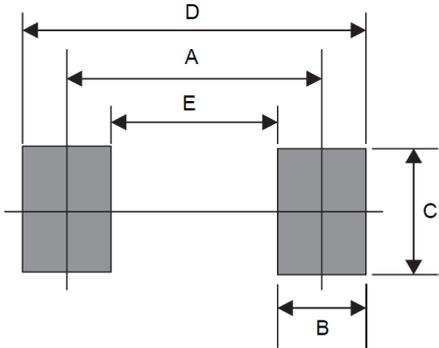


Note: Data is taken with a 10x attenuator

Fig 6. ESD Clamping Voltage 8 kV Contact per IEC61000-4-2

Suggested PAD Layout

Symbol	DFN1006-2L	
	(mm)	(inch)
A	0.70	0.028
B	0.40	0.016
C	0.60	0.024
D	1.10	0.043
E	0.30	0.012



The diagram illustrates the pad layout for the DFN1006-2L package. It shows two rectangular pads. Dimension A is the distance between the inner edges of the pads. Dimension B is the width of each pad. Dimension C is the height of each pad. Dimension D is the total distance between the outer edges of the pads. Dimension E is the distance between the inner edges of the pads, which is equal to A.

Marking Code

Part Number	Marking Code
STCDS12BL	R12

R12

Ordering information

Part Number	Package	Base qty	Reel Size	Delivery mode
		(pcs)	(inch)	
STCDS12BL	DFN1006-2L	10,000	7	Tape and reel