

1-Line Ultra Low Capacitance Bi-directional TVS Diode

Features

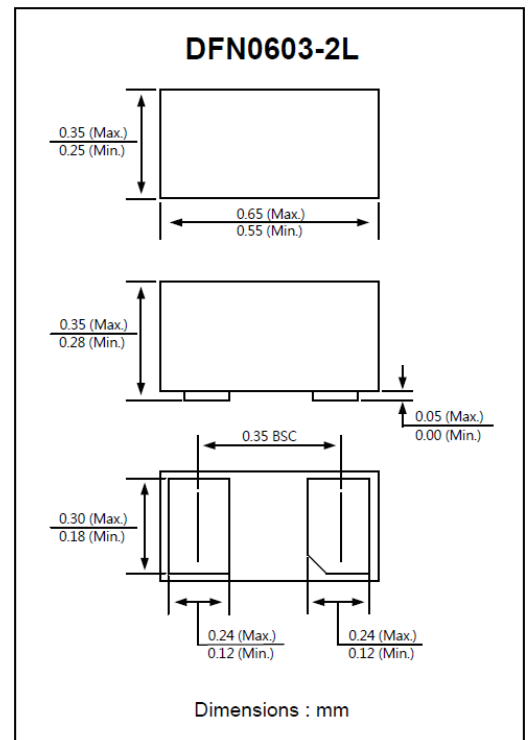
- IEC 61000-4-2 (ESD) $\pm 20\text{kV}$ (air), $\pm 20\text{kV}$ (contact)
- IEC 61000-4-5 (Lightning) 3A (8/20 μs)
- Ultra small package: 0.6x0.3x0.3mm
- Ultra low capacitance: 0.15pF typical
- Response time is typically <1ns
- Low clamping voltage
- 2-pin leadless package

Applications

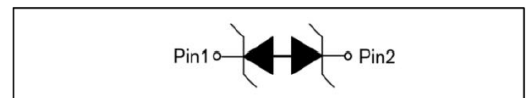
- Cellular Handsets and Accessories
- Display Ports
- MDDI Ports
- USB Ports
- Digital Visual Interface (DVI)
- PCI Express and Serial SATA Ports

Mechanical Characteristics

- Package: DFN0603-2L (0.6x0.3x0.3mm)
- Moisture Sensitivity: Level 1 per J-STD-020
- Qualified max reflow temperature 260°C
- Material: RoHS compliant



Circuit diagram



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless otherwise noted)

Parameter	Symbol	Value	Unit
Peak Pulse Power ($t_p = 8/20\mu\text{s}$)	P_{PP}	50	W
Peak Pulse Current ($t_p = 8/20\mu\text{s}$)	I_{PP}	3	A
ESD per IEC 61000-4-2 (Air)	V_{ESD}	± 20	KV
ESD per IEC 61000-4-2 (Contact)		± 20	KV
Lead Soldering Temperature	T_L	260 (10 sec)	$^\circ\text{C}$
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to + 150	$^\circ\text{C}$

Electrical Parameters ($T_A = 25^\circ\text{C}$ Unless otherwise noted)

Symbol	Parameter
I_{PP}	Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Reverse Stand-Off Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current

Electrical Characteristics ($T_A = 25^\circ\text{C}$ Unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Reverse Standoff Voltage	V_{RWM}				5	V
Reverse breakdown Voltage	V_{BR}	$I_T = 1\text{mA}$	6			V
Reverse leakage current	I_R	$V_{RWM} = 5\text{V}$			1.0	μA
Clamping Voltage	V_C	$I_{PP} = 1\text{A}, t_p = 8/20\mu\text{s}$			13	V
Clamping Voltage	V_C	$I_{PP} = 3\text{A}, t_p = 8/20\mu\text{s}$			17	V
Junction capacitance	C_J	$V_R = 0\text{V}, f = 1\text{MHz}$		0.15	0.23	pF

Typical Performance Characteristics ($T_A = 25^\circ\text{C}$ Unless otherwise noted)

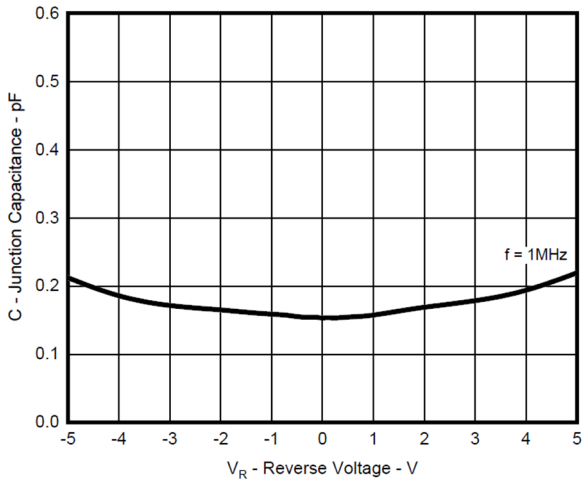


Fig 1. Junction Capacitance vs. Reverse Voltage

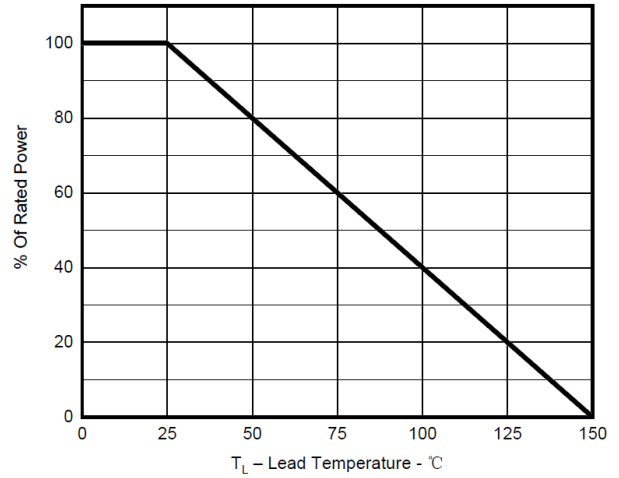


Fig 2. Power Derating Curve

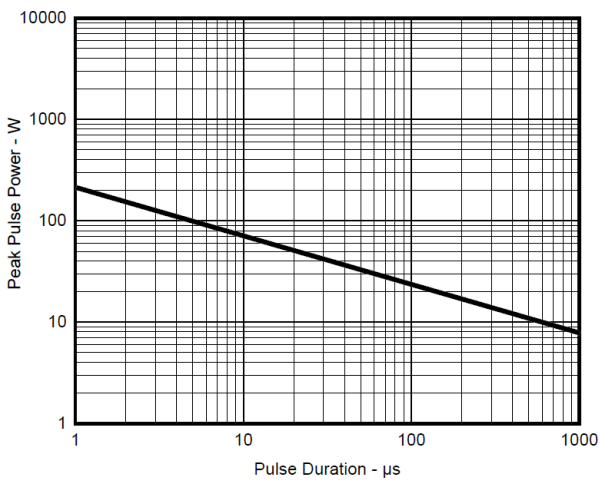


Fig 3. Peak Pulse Power Vs Pulse Time

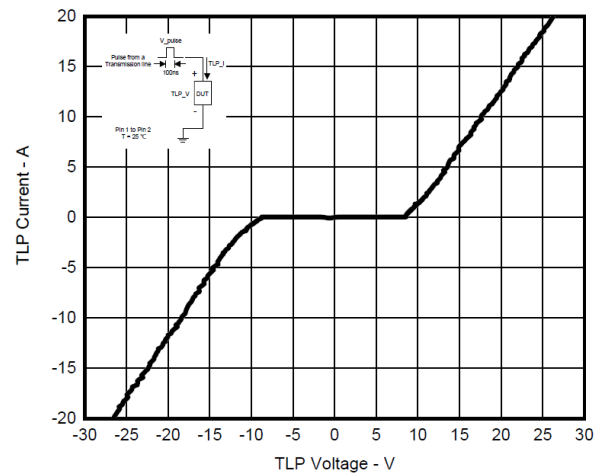


Fig 4. TLP Measurement

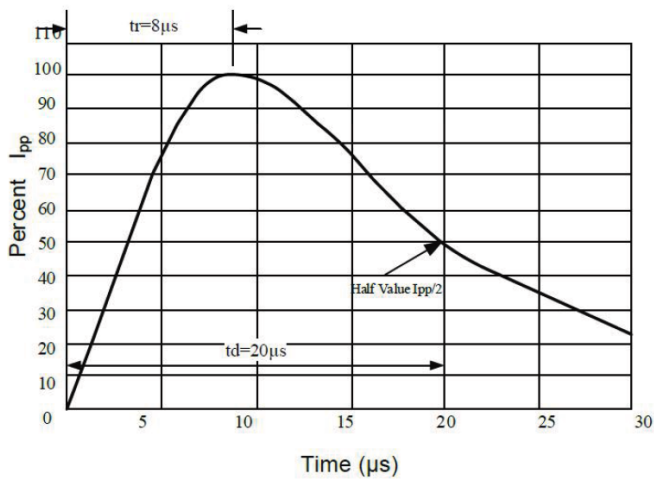
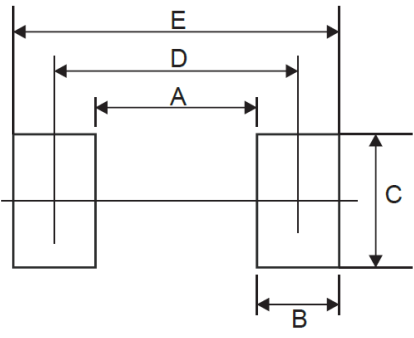


Fig 5. 8 X 20 μs Pulse Waveform

Suggested PAD Layout

Symbol	DFN0603-2L	
	(mm)	(inch)
A	0.15	0.006
B	0.25	0.010
C	0.32	0.013
D	0.40	0.016
E	0.65	0.026



The diagram illustrates the suggested pad layout for the DFN0603-2L package. It shows two rectangular pads. Dimension A is the distance between the inner edges of the pads. Dimension B is the width of the right pad. Dimension C is the height of the pads. Dimension D is the distance between the outer edges of the pads. Dimension E is the total width of the two pads including the gap between them.

Marking Code

Part Number	Marking Code
STED6050LP	UB

UB

Ordering information

Part Number	Package	Base qty	Reel Size	Delivery mode
		(pcs)	(inch)	
STED6050LP	DFN0603-2L	12,000	7	Tape and reel